Customer No.: 31561
Application No: 10/709,719
Docket No.:13114-US-PA

REMARKS

Present Status of the Application

This is a full and timely response to the outstanding final Office Action mailed on March 1, 2006. The Office Action has rejected claims 34-36, 38, 43, 46-49 under 35 U.S.C. 102(b) as being anticipated by Kim et al. (USP 5,252,845). The Office Action has further rejected claims 39-42, 44-45, 50-51 under 35 U.S.C. 103(a) as being unpatentable over Kim in view of Hisamoto et al. (USP IEDM 91).

Applicant has most respectfully considered the remarks set forth in this Office Action. Regarding the obvious rejections, it is however strongly believed that the cited references are deficient to adequately teach the claimed features as recited in the presently pending claims. The reasons that motivate the above position of the Applicant are discussed in detail hereafter, upon which reconsideration of the claims is most earnestly solicited.

Discussion of Office Action Rejections

The Office Action rejected claims 34-36, 38, 43, 46-49 under 35 U.S.C. 102 (b) as being anticipated by Kim et al. (US 5,252,845, Kim hereinafter).

Applicants respectfully assert that Kim is legally deficient for the purpose of anticipating claims 34 and 46 for the reasons that each and every element of the claims in issue is not found in the prior art reference.

The present invention teaches substantially, among other things, in claims 34 & 46 "*...defining an active area over the substrate to form a semiconductor pillar beside the deep trench capacitor and to form an isolation area;...*". On the other hand, Kim teaches forming an oxide layer 111 above the polysilicon 110 (Figure 5g), followed by forming silicon crystal 113 outside the trench by SEG process (Figure 5h). In other words, the alleged pillar 113 and isolation area of Kim are formed in different steps. Further, the alleged pillar 113 of Kim is a silicon layer formed above the substrate 101 outside the trench (col. 4, ln. 41-46, Figure 5h) and is not formed from a part of the substrate 101. The semiconductor pillar of the instant case, however, is defined from the substrate and is formed from a part of the substrate.

Additionally, claims 38 and 43 details the steps of forming the gate dielectric layer and the word line including the treble gate in which the steps include filling the isolation area with an insulating material; patterning the insulating material to expose a first sidewall of the pillar above a predetermined level and ...". There is nowhere in Kim that either explicitly teaches or implicitly suggests filling an isolation area with an insulating material or pattering the insulating material. Instead, the formation of the gate dielectric layer and the word line of Kim includes forming a gate oxide layer 115 over the silicon crystal 113 that is formed on the substrate 100 and over the polysilicon 110 that fills the trench, followed by forming the word line 116 on a part of the gate oxide layer that is over the polysilicon 110.

For at least these reasons, Applicant respectfully asserts that Kim fails to teach or suggest the present invention or to render claims 34 or 46 anticipated. Since claims 35-36, 38-45 &

claim 47-51are dependent claims, which further define the invention recited in claims 34 and 46, respectively. Applicants respectfully assert that these claims also are in condition for allowance. Thus, reconsideration and withdrawal of this rejection are respectfully requested.

The Office Action rejected claims 39-42, 44-45 and 50-51 under 35 U.S.C. § 103(a) as being unpatentable over Kim in view of Hisamoto et al.(IEDM 91, Hisamoto hereinafter).

With regard to the 103 rejections of claims by Kim in view of Hisamoto, Applicants respectfully submit that these claims defined over the prior art references for at least the reasons discussed above.

Moreover, Hisamoto teaches that the upright ultra-thin Si layer is covered by the word-line and **the storage node is stacked on these structures**. See Figure 1. On the other hand, Claims 34 and 46 of the present invention specifically teaches the semiconductor pillar is formed beside the capacitor, and the word line 948, 1820, 2240 is formed above than the capacitor 910. In essence, Hisamoto teaches away the present invention, the motivation to combine Kim with Hisamoto is thus lacking.

For at least the reason set forth hereinbefore, Applicants submit that the rejections to claims 39-42, 44-45 and 50-51 have been traversed, rendered moot, and/or accommodated, and that the pending claims 39-42, 44-45 and 50-51 are in condition for allowance. Favorable consideration and allowance of the present application and all pending claims are hereby courteously requested.

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CONCLUSION

For at least the foregoing reasons, it is believed that the presently pending claims 34-36, 38-51, are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

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Respectfully submitted,

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